CLAIMS

What is claimed is:

1. A feedforward equalizer for equalizing a sequence of signal samples received from a remote transmitter, the feedforward equalizer having a gain and being included in a receiver, the receiver having a timing recovery module for setting a sampling phase and a decoder, the feedforward equalizer comprising:

(a) a non-adaptive filter receiving the signal samples and producing a filtered signal; and

(b) a gain stage coupled to the non-adaptive filter, the gain stage allowing adjustment of the gain of the feedforward equalizer by adjusting the amplitude of the filtered signal, the amplitude of the filtered signal being adjusted so as to fit in operational range of the decoder;

wherein the feedforward equalizer does not affect the sampling phase setting of the timing recovery module of the receiver.

2. The feedforward equalizer of claim 1 wherein the feedforward equalizer does not enhance noise.

3. The feedforward equalizer of claim 1 wherein the non-adaptive filter produces a precursor included in the filtered signal, the precursor being an indicator preceding each of the signal samples to facilitate timing recovery.

4. The feedforward equalizer of claim 3 wherein the non-adaptive filter is a finite impulse response filter having a transfer function of the form $-\gamma + z^{-1}$, where γ is a programmable constant.

5. The feedforward equalizer of claim 4 wherein γ is equal to 1/16 when the receiver is connected to the remote transmitter by a cable having a length of less than eighty meters.

6. The feedforward equalizer of claim 4 wherein γ is equal to 1/8 when the receiver is connected to the remote transmitter by a cable having a length of more than eighty meters.

7. The feedforward equalizer of claim 1 wherein the non-adaptive filter substantially eliminates from the received signal samples intersymbol interference introduced by pulse shaping at the remote transmitter.

8. The feedforward equalizer of claim 7 wherein the non-adaptive filter is an infinite impulse response filter having a transfer function of the form $1/(1 + z^{-1}K)$, where K is a programmable constant.

9. The feedforward equalizer of claim 8 wherein K is equal to a value less than 1 during start-up of the receiver and is slowly decreased to 0 after a criterion is satisfied.

10. The feedforward equalizer of claim 9 wherein the criterion is convergence of a decision-feedback equalizer included in the decoder.

11. The feedforward equalizer of claim 1 wherein adjustment of the gain of the feedforward equalizer is programmable.

12. The feedforward equalizer of claim 1 wherein the gain stage includes an adaptation circuit to adaptively adjust the gain of the feedforward equalizer based on gain-adjusting inputs received from the decoder.

13. The feedforward equalizer of claim 12 wherein the gain-adjusting inputs are a tentative decision and an associated error.

14. The feedforward equalizer of claim 12 wherein the adaptation circuit comprises no actual multiplier.

15. The feedforward equalizer of claim 1 further comprises a noise cancellation stage, the noise cancellation stage subtracting from the filtered signal a noise signal received from a noise computing module of the receiver and producing a noise-reduced filtered signal.

16. The feedforward equalizer of claim 15 wherein the noise cancellation stage is disposed between the non-adaptive filter and the gain stage and provides the noise-reduced filtered signal to the gain stage, the location of the noise cancellation stage allowing the noise signal to be substantially unaffected by the gain of the feedforward equalizer.

17. A method for equalizing a sequence of input samples received at a receiver from a remote transmitter, the receiver having a timing recovery module for setting a sampling phase and a decoder, the method comprising the operations of:

(a) filtering the input samples using a non-adaptive filter to produce a filtered signal; and

(b) adjusting the amplitude of the filtered signal so that the amplitude of the filtered signal fits in operational range of the decoder;

wherein operations (a) and (b) do not affect the sampling phase setting of the timing recovery module of the receiver.

18. The method of claim 17 wherein operations (a) and (b) do not amplify noise.

19. The method of claim 17 wherein operation (a) includes the operation of providing a precursor in the filtered signal, the precursor being an indicator preceding each of the signal samples in the filtered signal to facilitate timing recovery.

20. The method of claim 19 wherein the non-adaptive filter is a finite impulse response filter having a transfer function of the form $\gamma + z^{-1}$, where γ is a programmable constant.

21. The method of claim 20 wherein γ is equal to 1/16 when the receiver is connected to the remote transmitter by a short cable.

22. The method of claim 20 wherein γ is equal to 1/8 when the receiver is connected to the remote transmitter by a long cable.

23. The method of claim 17 wherein operation (a) includes the operation of substantially eliminating from the received signal samples intersymbol interference introduced by pulse shaping at the remote transmitter.

24. The method of claim 23 wherein the non-adaptive filter is an infinite impulse response filter having a transfer function of the form $1/(1+z^{-1}K)$, where K is a programmable constant.

25. The method of claim 24 wherein K is equal to a value less than 1 during start-up of the receiver and is slowly decreased to 0 after a criterion is satisfied.

26. The method of claim 25 wherein the criterion is convergence of a decision-feedback equalizer included in the decoder.

27. The method of claim 1 wherein adjustment of the amplitude of the filtered signal is programmable.

28. The method of claim 1 wherein operation (b) is performed via a gain stage, the gain stage including an adaptation circuit to adaptively adjust the amplitude of the filtered signal based on gain-adjusting inputs received from the decoder.

29. The method of claim 28 wherein the gain-adjusting inputs are a tentative decision and an associated error.

30. The method of claim 28 wherein the adaptation circuit comprises no actual multiplier.

31. The method of claim 17 further comprises the operation of:

(c) producing a noise-reduced filtered signal by subtracting from the filtered signal a noise signal received from a noise computing module of the receiver.

32. The method of claim 31 wherein operation (c) is performed prior to operation (b), the ordering of operations (c) and (b) allowing the noise signal to be substantially unaffected by operation (b).

33. A system for demodulating a sequence of input samples received from a remote transmitter, the system being included in a receiver, the receiver having a timing recovery module for setting a sampling phase, the system comprising:

(a) a feedforward equalizer having a gain, receiving and equalizing the input samples; and

(b) a decoder system coupled to the feed-forward equalizer to receive and decode the equalized input samples;

wherein the feedforward equalizer does not affect the sampling phase setting of the timing recovery module of the receiver.

34. The system of claim 33 wherein the feedforward equalizer comprises:

(a) a first filter receiving the input samples and generating a first signal, the first signal including a precursor, the precursor being an indicator preceding each of the input samples to facilitate timing recovery;

(b) a second filter coupled to the first filter, the second filter compensating intersymbol interference included in the first signal and producing a second signal;

(c) a noise cancellation stage coupled to the second filter, the noise cancellation stage receiving the second signal from the second filter and a noise signal from a noise computing module of the receiver, the noise cancellation stage subtracting the noise signal from the second signal and producing a third signal; and

(d) a gain stage coupled to the noise cancellation stage, the gain stage providing adjustment of the gain of the feedforward equalizer by adjusting the amplitude of the third signal, the amplitude of the third signal being adjusted so as to fit in operational range of the decoder.

35. The system of claim 34 wherein the feedforward equalizer does not amplify noise.

36. The system of claim 34 wherein each of the elements (a), (b), (c) and (d) of the feedforward equalizer has an output and includes a register proximate of the respective output to prevent computational delay from one of the elements to propagate to a succeeding element.

37. The system of claim 34 wherein the precursor filter is a finite impulse response filter having a transfer function of the form $-\gamma + z^{-1}$, where γ is a programmable constant.

38. The system of claim 34 wherein γ is equal to 1/16 when the receiver is connected to the remote transmitter by a short cable.

39. The system of claim 34 wherein γ is equal to 1/8 when the receiver is connected to the remote transmitter by a long cable.

40. The system of claim 34 wherein the second filter is an infinite impulse response filter having a transfer function of the form $1/(1 + z^{-1}K)$, where K is a programmable constant.

41. The system of claim 40 wherein K is equal to a value less than 1 during start-up of the receiver and is slowly decreased to 0 after a criterion is satisfied.

42. The system of claim 41 wherein the criterion is a convergence of a decision-feedback equalizer included in the decoder system.

43. The system of claim 34 wherein the gain stage includes an adaptation circuit to adaptively adjust the gain of the feedforward equalizer based on gain-adjusting inputs received from the decoder system.

44. The system of claim 43 wherein the gain-adjusting inputs are a tentative decision and an associated error.

45. The system of claim 43 wherein adjustment of the gain of the feedforward equalizer is programmable.

46. The system of claim 43 wherein the adaptation circuit comprises no actual multiplier.

47. The system of claim 33 wherein the system comprises L identical feedforward equalizers operating in parallel, each of the L feedforward equalizers providing an equalized input sample to the decoder system, the L equalized input samples forming an L-dimensional sample, the decoder system decoding the L-dimensional sample into a final decision corresponding to a codeword of a trellis code having N states.

48. The system of claim 47 further comprises a de-skew memory module, the de-skew memory module aligning the L equalized input samples according to a de-skew control signal and providing the L aligned input samples to the decoder system.

49. The system of claim 47 wherein the decoder system comprises:

(1) a decoder block decoding a set of signal samples to generate tentative decisions and the final decision;

(2) a decision-feedback equalizer coupled to the decoder block to receive the tentative decisions, the decision feedback equalizer having a set of low-ordered coefficients and a set of high-ordered coefficients, the decision-feedback equalizer generating a tail value based on the tentative decisions and values of the high-ordered coefficients; and

(3) a multiple decision feedback equalizer coupled to the decision-feedback equalizer to receive the tail value and values of the low-ordered coefficients, the multiple decision feedback equalizer receiving the L-dimensional sample and generating the set of signal samples for the decoder block.

50. The system of claim 49 wherein the decoder block comprises:

a Viterbi decoder, the Viterbi decoder receiving the set of signal samples and computing path metrics for each of the N states of the trellis code and outputs decisions based on the path metrics; and

a path memory module coupled to the Viterbi decoder to receive the decisions, the path memory module having a number of depth levels corresponding to consecutive time instants, each of the depth levels including N registers for storing decisions corresponding to the N states, each of selected depth levels including a multiplexer for selecting a best decision from corresponding N registers, the best decision at the last depth level being the final decision, the best decisions at other selected depth levels being the tentative decisions.

51. The system of claim 49 wherein each of the tentative decisions corresponds to a codeword of the trellis code.

52. The decision-feedback sequence estimation block of claim 49 wherein the decision-feedback equalizer includes a delay line and the tentative decisions are inputted into the decision-feedback equalizer at various locations of the delay line.

53. The decision-feedback sequence estimation block of claim 50 wherein the tentative decisions are generated from the first three depth levels of the path memory module.

54. The decision-feedback sequence estimation block of claim 49 wherein the set of low-ordered coefficients comprises the first two coefficients of the decision-feedback equalizer.

55. The decision-feedback sequence estimation block of claim 49 wherein the multiple decision feedback equalizer comprises:

(a) a computing module generating a set of pre-computed values based on the values of the low-ordered coefficients;

(b) a set of adders coupled to the computing module, the adders corresponding one-to-one to the pre-computed values, each of the adders combining the corresponding pre-computed value with the tail value to generate a tentative sample; and

(c) N multiplexers corresponding to the N states of the trellis code, each of the N multiplexers being coupled to the adders to receive the tentative samples, each of the N multiplexers selecting and outputting one of the received tentative samples as one of the signal samples to the decoder.

56. The decision-feedback sequence estimation block of claim 55 wherein the multiple decision feedback equalizer further comprises:

(d) a set of registers coupled to the set of adders to receive the tentative samples, the registers being located between the adders and each of the N multiplexers, the registers providing the tentative samples to the multiplexers;

wherein the locations of the registers facilitate high-speed operation by breaking up a critical path of computations into substantially balanced first and second portions, the first portion including computations in the decision-feedback equalizer and the multiple decision feedback equalizer, the second portion including computations in the decoder.

57. The decision-feedback sequence estimation block of claim 56 wherein the multiple decision feedback equalizer further comprises a set of saturators coupled to the set of adders to receive the tentative samples, the saturators saturating the tentative samples and providing the saturated tentative samples to the registers.

58. The decision-feedback sequence estimation block of claim 55 wherein the pre-computed values are based on values of the set of low-ordered coefficient and known symbol values.

59. The decision-feedback sequence estimation block of claim 55 wherein each of the N multiplexers selects one of the received tentative samples based on a decision received from the decoder.